

## Computer Organization And Architecture Solutions Linda Null

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Computer Organization & Architecture SOLUTION INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INR signal & activates INTA signal, so another request can't be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option. Question. 12

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where the problem size is increased with the machine size so that the solution time is the same for sequential and parallel executions. 2.6 a. Say Program P1 consists of n x86 instructions, and hence 1.5 x n MIPS instructions. Computer A operates at 2.5 GHz, i.e. it takes 0.4ns per clock. So

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Design constraints on a computer's memory can be summed up by three questions: How much, how fast, how expensive There is a trade-off among capacity, access time, and cost Faster access time, greater cost per bit Greater capacity, smaller cost per bit Greater capacity, slower access time The way out of the memory dilemma is not to rely on a ...